78470PCW
Customer No. 01333

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Robert M. Guidash

IMPROVED LINEARITY AND DYNAMIC RANGE FOR COMPLEMENTARY METAL OXIDE SEMICONDUCTOR ACTIVE PIXEL IMAGE SENSORS

Serial No. US 09/750,745

Filed 29 December 2000

Group Art Unit: 2877

Examiner: Nguyen, Tu T.

I hereby certify that this correspondence is being deposited today with the United States Postal Service as first class mail in an envelope addressed to Commissioner for Patents, Washington, D.C. 20231.

Lois A. Massar

Date

Commissioner for Patents
Washington, D.C. 20231

Sir:

DECLARATION UNDER 37 CFR 1.132

Robert M. Guidash declares that he is the inventor of the subject application; that he conceived his invention in this country on November 14, 1997 which is long prior to Aug. 16, 1999 (hereinafter the effective date); that he realized his work as being inventive on May 28, 1998; that he submitted an invention disclosure (enclosed herewith) on October 20, 1998; that it was approved by management on October 23, 1998; that to the best of his knowledge, Jim Leimbach, the Eastman Kodak Attorney (no longer employed with Eastman Kodak Company), diligently attempted to progress through his docket to start working on the subject invention; that, to the best of his knowledge, Jim Leimbach realized his docket prevented him from working on it in a desired time; that Jim Leimbach sent the subject application to an outside attorney, Fred Gibbs, on March 7, 2000; that there was numerous correspondence with Fred Gibbs on the subject patent application; that he responded diligently to the correspondence; that, to the best of his knowledge, Fred Gibbs worked substantially continuously on the subject patent application after he received it; and that he does not believe that his invention has been in public prior to his application; and that he has never abandoned the invention.

He further declares that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Respectfully Submitted,

_____

Robert M. Guidash

INV... ...ION SUMMARY FOR IP COORDINA...

SEND TO: IP Coordinator

Instructions: If drawings or other additional information are needed to describe the invention, or if prior art is being submitted, fill out this form, print it, attach copies and mail to your Intellectual Property (IP) Coordinator.

THIS SECTION TO BE COMPLETED BY IP COORDINATOR*

Date Received: 10/22/98 Proceed to Patent: X Yes ___ No

Approved: David N Nichols Approval Date: 10/23/98
IP Coordinator

PRE-FILING EVALUATION
(See IP Subcommittee Guidelines for more detailed rating criteria)

Internal Use (1 = low, 10 = high) 7
External Use (1 = low, 10 = high) 8
Detectability (.5 = nondetectable, 1.0 = easy to detect) 0.8

Docket No.: 78470 Docket Date: 9/25/98
Portfolio No. ________ Date Filed in USPTO: ________

*For record keeping, send copies of this form to inventor(s) & attorney.

Earliest date of invention: 11/14/97
Date when realized as patentable invention: 5/22/98

Inventors: R MICHAEL GUIDASH

Documention: (Notebook No./Page No., Other (e.g., Technical Reports, Memos, Make Sheets, etc.) (1) PC files, MIKE/ACI/TV2DATA/cdr-lin.xls
(2) Design files; mcl/layout/test... /cdr-lin
(3) Note book AA5962 pg. 48-50

Title of Invention: Improved Linearity for CMOS APS

Summary of Invention: (See attached documentation)

- Reduces or minimizes ratio of voltage dependent capacitance to total sense node capacitance so more linear across voltage range.

(1) Minimize junction capacitance of floating diffusion
(2) Add voltage independent capacitance to sense node
(3) Use common source configuration

October 20, 1998

INVENTION SUMMARY FOR IP COORDINATOR (Continued)

Advantages: • Improved linearity
• Lower Gain FPN

Limitations: • None envisioned

Why this invention should be patented: Higher quality, low cost CMOS Active Pixel Sensors

Has the invention been reduced to practice? ✓ Yes ___ No Where, when?

Has the invention been disclosed to the public or offered for sale? ___ Yes ✓ No
Where, when?

RESEARCH LABORATORY
EASTMAN KODAK COMPANY

Notebook No. AA 5962

Date 5/28/98

Problem: Improved linearity for CMOS Active Pixel Sensors

In CMOS active pixel sensors made in sub-µ CMOS processes, and scaled supply voltages, it is typical that the capacitance used to convert signal electrons to a voltage has a large voltage coefficient. This is due to the a) large ratio of junction capacitance to interconnect and other gate capacitance components, and b) the change in the junction depletion region ~~as~~ from full well swing is large compared to the nominal depletion region width.

In addition the charge to voltage conversion of transfer gated pixels with an isolated charge sense node (i.e. separate from the photodetector), is very high (> 50 µV/e⁻ typically), and can limit the saturation signal level.

There are ways proposed here to mitigate these problems -

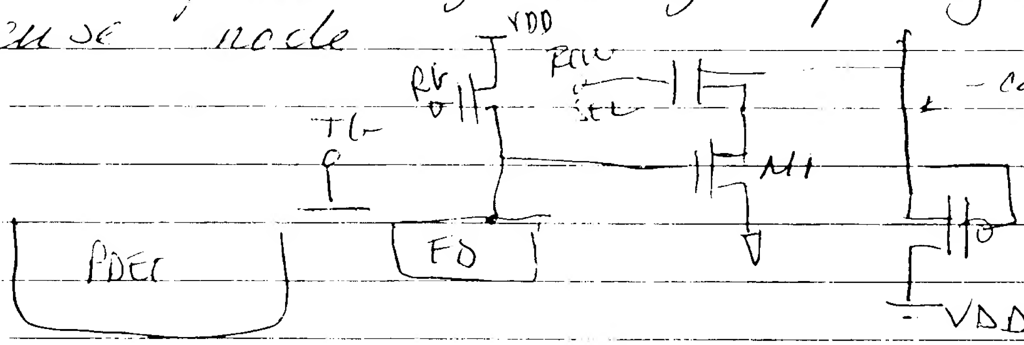
(1) Use a common source amplifier as the read out mechanism, rather than a source follower. (see FIG 1)

In this case the gain of a common source amplifier can be made arbitrarily large

Signature [signature]

The foregoing disclosed to me on Aug 28 1998 David H Sackett
Witness

so that the sense node junction capacitance is a smaller component of the overall capacitance to improve linearity, and so the total capacitance is larger to provide larger charge capacity on the sense node



(FIG. 1)

Note the same scheme in FIG 1 can be used with a standard Photodiode detector (i.e. no TG). The Cin can be made (selected) larger by designing the common-source gain to provide the desired Miller effect on the Cgd and Cg channel of the in pixel input transistor.

$$C_{in_{M1}} = (1 - A_v) C_{gd}'$$

(2) Use poly-poly or other electrode-electrode capacitor connected to the sense node. This capacitance has a very low V coefficient and improves linearity and charge capacity

Signature K. Michael Benchek

The foregoing disclosed to me on May 22 1998 David A. Sackett
Witness

GE
0

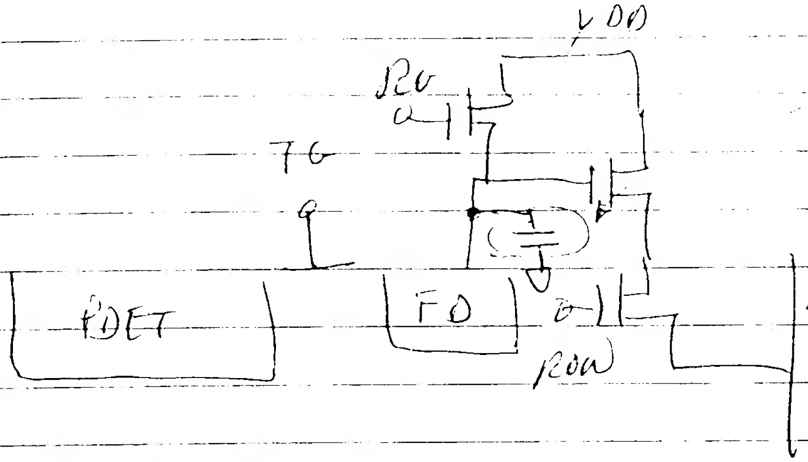
RE ARCH LABORATORI
EASTMAN KODAK COMPANY

Notebook No. AA 5962

te 5/28/98

blem: Improved linearity . . .

- for the same reasons stated in approach #1.
(see FIG. 2)



poly to poly* Capacitor

column bus

* or poly-metal Capacitor, or gate-substrate capac.
or metal-metal etc

KP 15226-B I.P.S.

Signature [signature]

The foregoing disclosed to me on May 28 1998 David N. Sackett
Witness